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Giant step-bunching occurrence during graphene growth on 4H-SiC(0001)

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Motivations

The main obstacle to the use of graphene on the industrial scale is the growth of a large and homogenous monolayer graphene. Concerning this issue, it is worth noting that our group has recently developed a reproducible and controlled growth process of a monolayer graphene on SiC(0001) by sublimation at low Ar pressure. i.e. 10 mbar [1]. Still, the control of the electronic properties of the obtained graphene by this process is very challenging. E.g. the mobility on our graphene on 4H-SiC(0001) is around 2000 $cm^2 v^{-1} s^{-1}$ at RT which is in the range of the measured mobilities on similar substrates [2]. Yet, it is still very low when compared with the mobilities reported for suspended graphene [3]. It is well accepted that the electronic properties of graphene on SiC are highly sensitive to the substrate underneath. It was reported that the mobility of graphene on SiC(0001) increases with increasing SiC steps width, and its resistance increases with increasing SiC steps height [4;5]. This means that the electronic properties of graphene on SiC(0001) can be tuned by controlling the height and width of the terraces that results from the surface reconstruction of SiC before the growth .i.e. Step bunching phenomenon.

State of the art : Step bunching on SiC(0001)

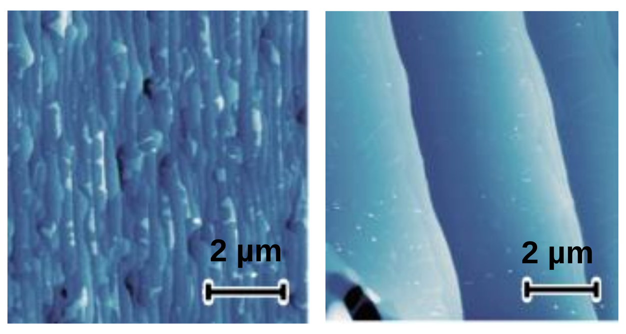
Movement of the surface atoms at high temperature and the formation of high steps and wide terraces

H. Matsunami et al, Materials Science and Engineering: R: Reports.1997, 20, 25–166

How to control step bunching on SiC(0001) ?

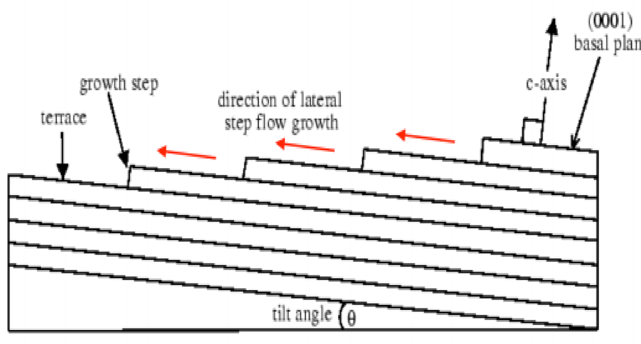
- **Temperature ramp**
- **Miscut angle (θ)**
- **H_2 etching**

1 °C/s 0.66 °C/s



Steps width increases with lowering the temperature ramp

Bao et al, Appl. Phys. Lett. 2016, 109, 081602



The width of terraces is sensitive to SiC miscut angle even if "small" (θ<0.1°)

Dimitrakopoulos et al, Appl. Phys. Lett. 2011, 98, 22105

- Remove polishing damages

G.R. Yazdi et al, Carbon. 2013, 57, 477–484

- Delay the buffer layer graphene formation

Kruskopf et al, Thin solid films. 2018, 659, 7-15

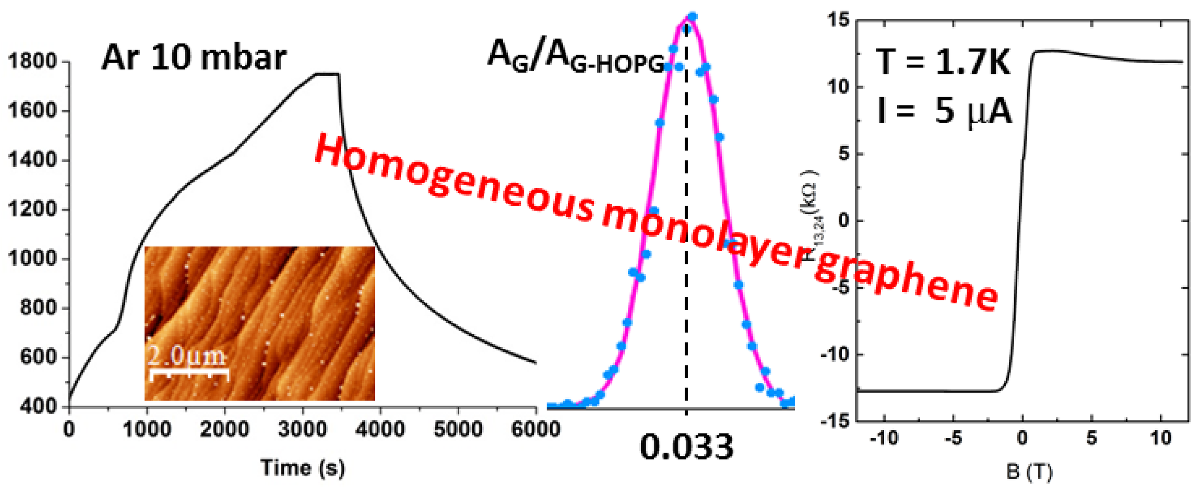
Our sublimation process to grow graphene

- **HTA-100 characteristics (prototype)**

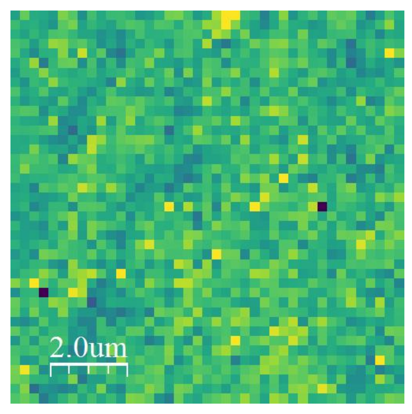
Gas lines: Ar, N_2, CH_4, C_2H_4, C_3H_8, H_2
Stainless steel water-cooled chamber
Up to 2000˚C
Ramp rate up to 10 ˚C/s
Vacuum range: Atmosphere to 10^{-6} Torr
Sublimation or CVD

https://www.annealsys.com/products/rtp-and-rtcvd/zenith-150.html

- **Growth process: 10 mbar, 1750˚C**



P. Landois et al , Phys. Chem. Chem. Phys., 2017, 19, 15833--15841
N. Camara, Phys. Rev. B, 2009, 80, 125410



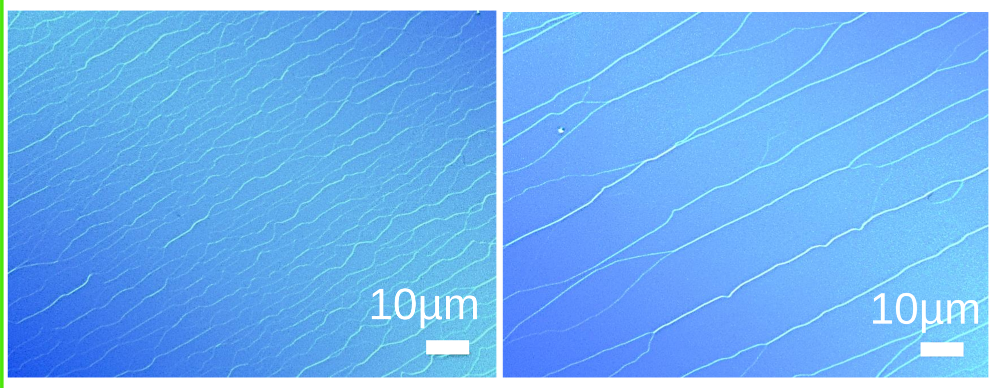
Raman map at 532 nm

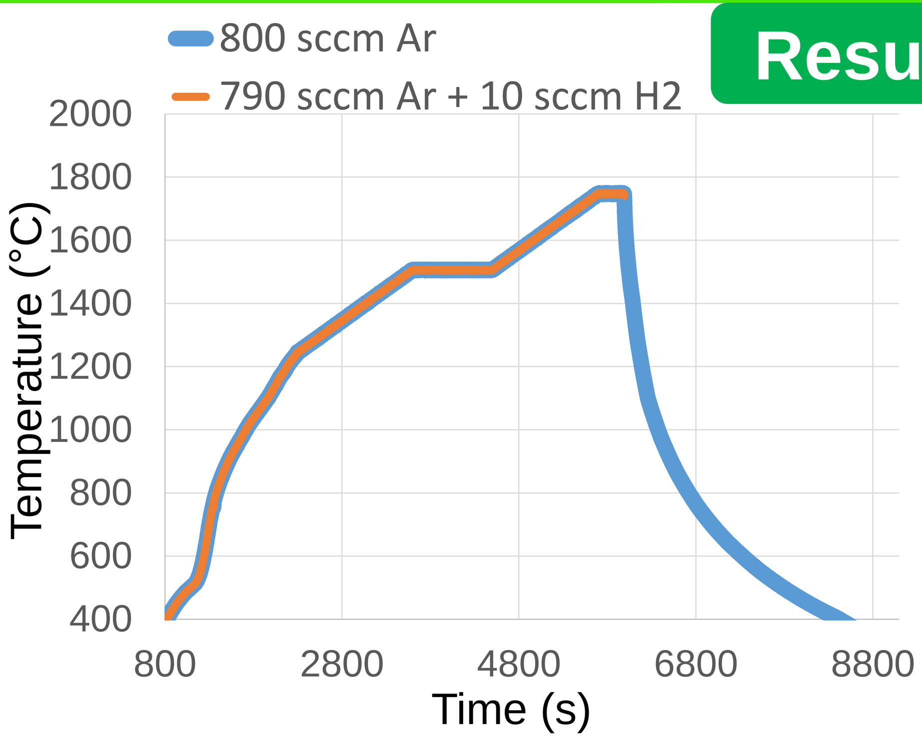
Results

H_2 etching

- Evidence of H_2 effect by MO (DIC)

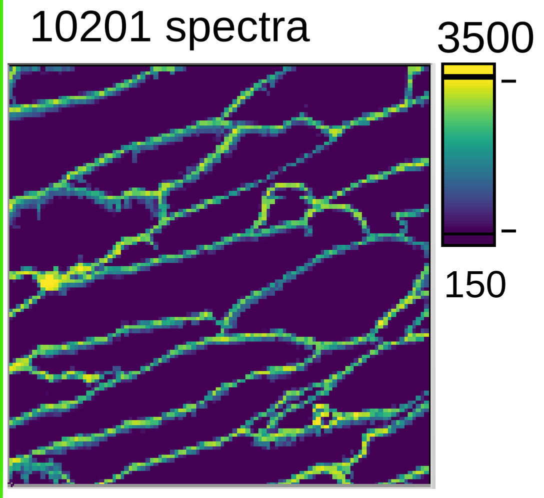
Without H_2 With H_2

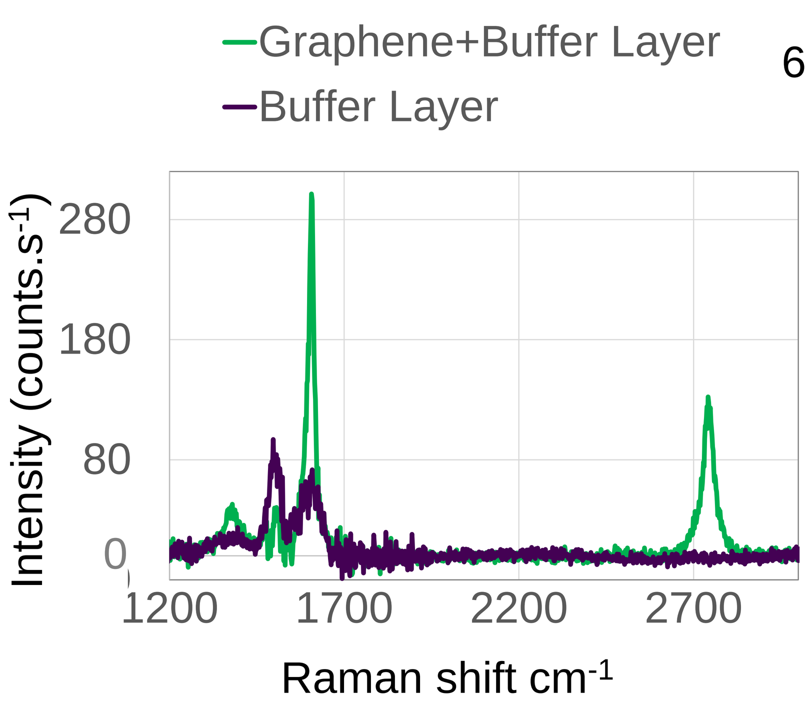


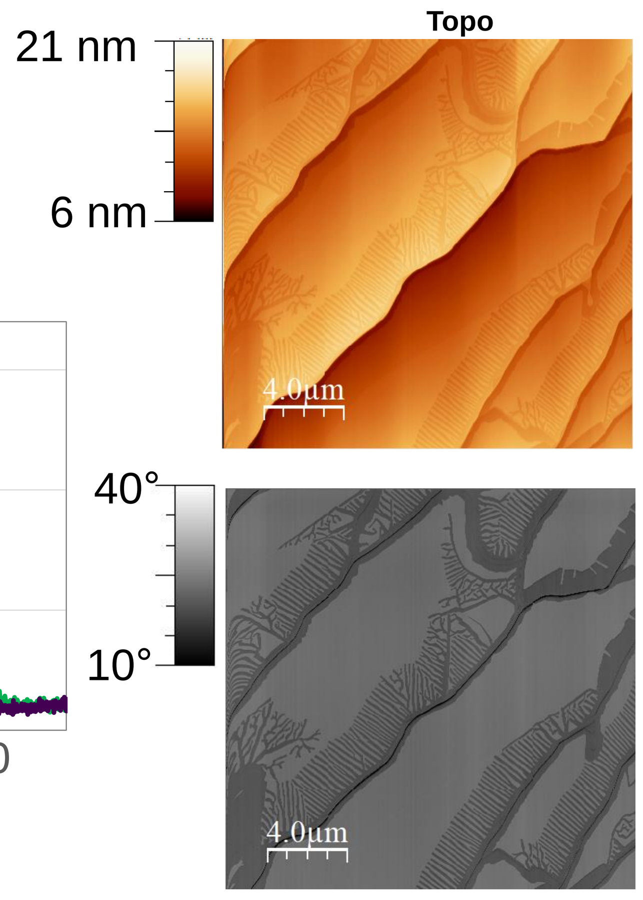


- Terraces characterizations: Raman and AFM, complementary technics

A_{2D} counts.s^{-1}.cm^{-1}
(50 µm x 50 µm)
10201 spectra





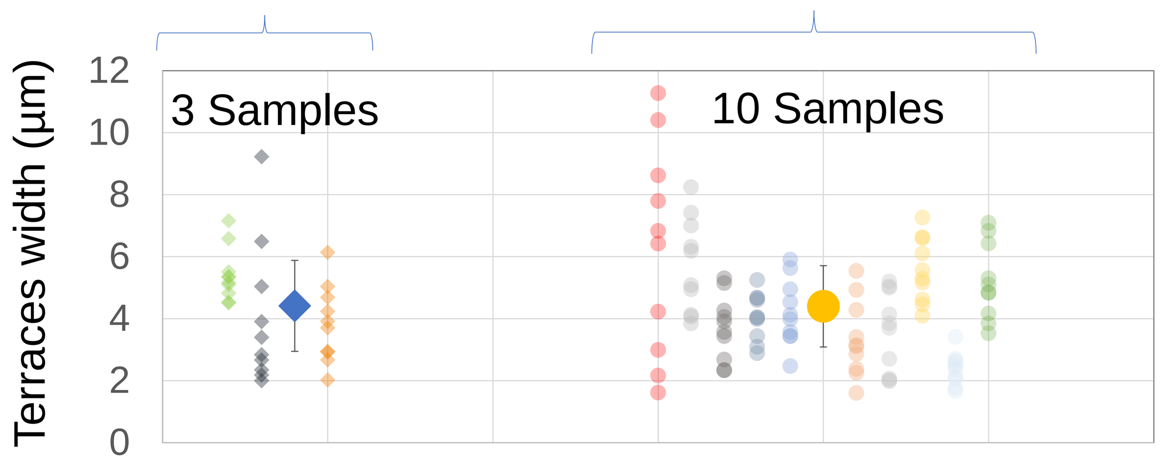


Large terraces up to 20 µm with H_2 covered with buffer layer
Graphene formation delayed

Wafer miscut Angle

Miscut uncertainty ~ 0.5°

Tankeblue, China



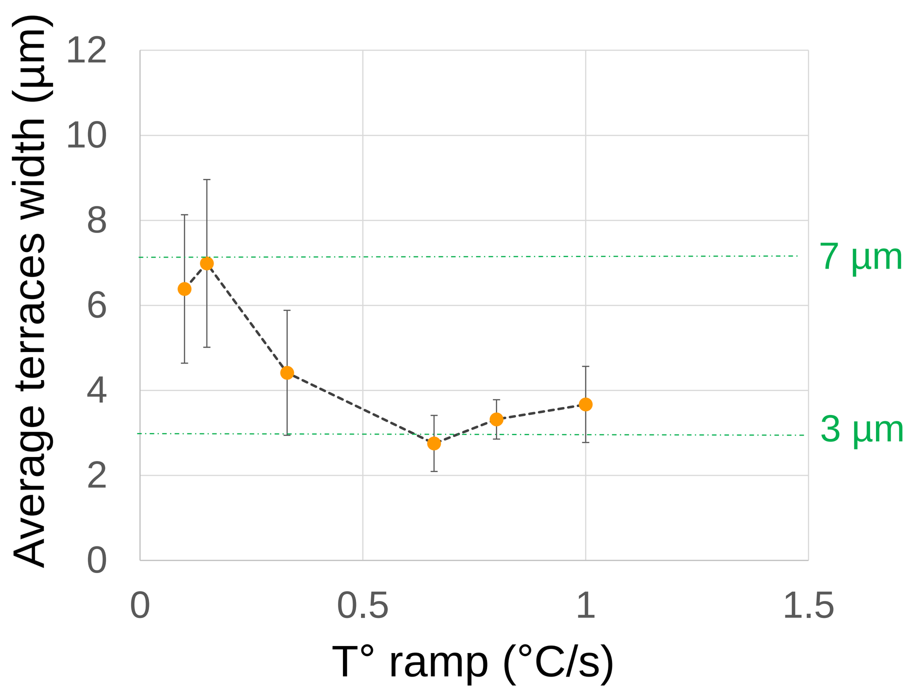
T ramp at 0.33°C/s, 10 mbar, 1740°C, 800 sccm Ar

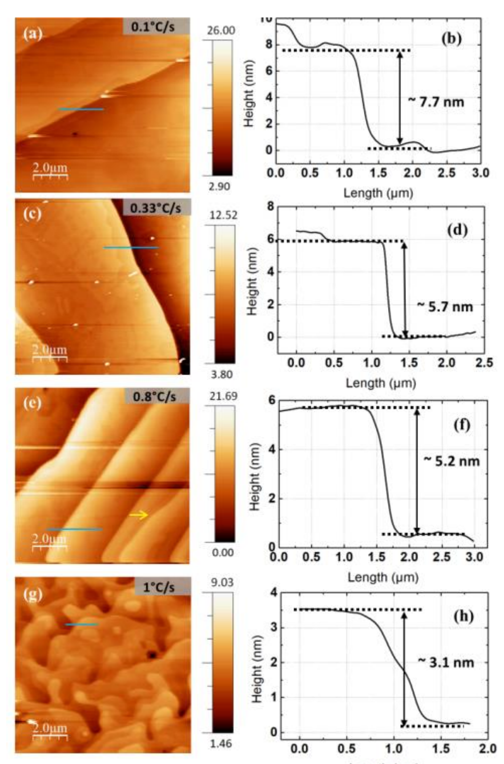
- Average Terraces width Wafer 1
- Average Terraces width Wafer 2

Both wafers are 4H-SiC(0001) on axis, no clear wafer effect
➡ Others 4H
➡ 4H vs 6H
➡ HR-XRD to determine the miscut with an uncertainty around 0.015

J Enslin et al Phys. Status Solidi A . 2019, 216, 1900682

Temperature ramp effect





Larger terraces at low T ramp confirming our previous results

Tianlin wang, thesis, University of Montpellier, 2018

Conclusions and perspectives

We have identified in the state of art the parameters allowing the control of step bunching on SiC(0001). We have started testing some of those parameters (temperature ramp, H_2 etching…) and regular steps with a width up to 20 µm have been obtained. As far as we know, our steps are by far larger than those reported in the literature i.e. 100 of nanometers to some µm. The main challenge now would be to cover the large steps by monolayer graphene. Once a reproducible and well controlled process is identified, we will measure the electronic properties of the obtained graphene. At the same time we are exploring some alternative ways to enhance the electronic properties of our graphene such as limiting the buffer layer effect and optimizing the growth on the C face of SiC.

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[3] H. Chang et al Adv. Funct. Mater. 2013, 23, 1984–1997
[4] Dimitrakopoulos et al Appl. Phys. Lett. 2011, 98, 222105
[5] F.M. Ross et al Nature Mater. 2012,11 114–119

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